Projektovanje digitalnih integrisanih kola

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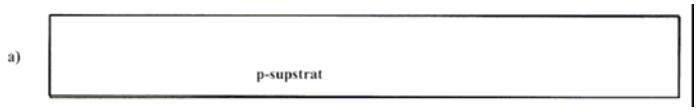
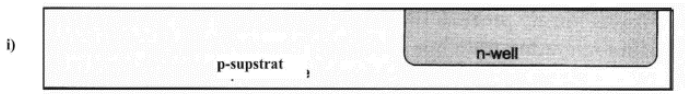
2.1 Osnovni CMOS proces

Pod *n-well* tehnologijom podrazumeva se proces koji se izvodi na supstratu p-tipa.



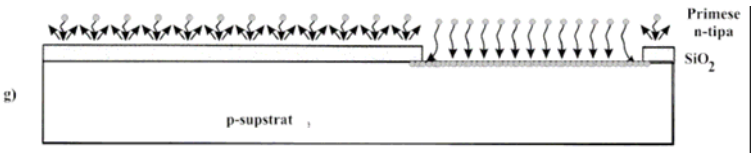
2.1 Osnovni CMOS proces

Da bi se u njemu formirao pMOS tranzistor, neophodno je da se u supstrat ugradi oblast n-tipa.



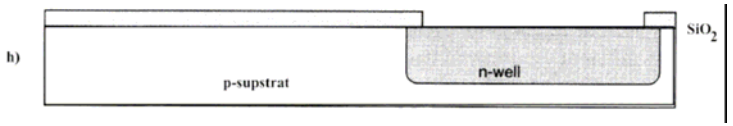
2.1 Osnovni CMOS proces

U tu svrhu, difuzijom ili jonskom implantacijom „napada“ se osnova donorskim primesama sve dok se ne promeni tip poluprovodnika.



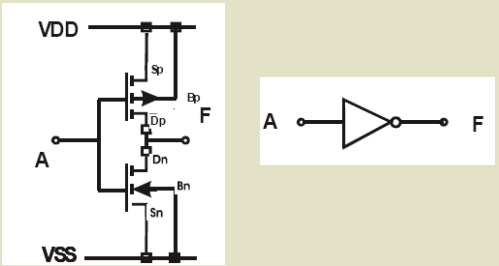
2.1 Osnovni CMOS proces

Kao rezultat nastaje struktura koja liči na jamu n-tipa u osnovi p-tipa. Odatle i originalni naziv n-*well*.



2.1 Osnovni CMOS proces

Primer invertor



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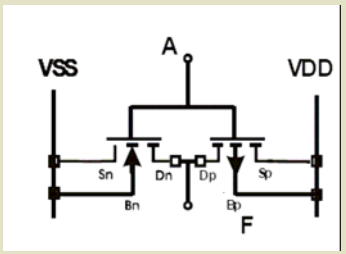
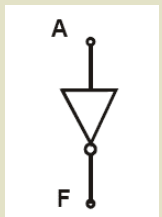
Primer invertor





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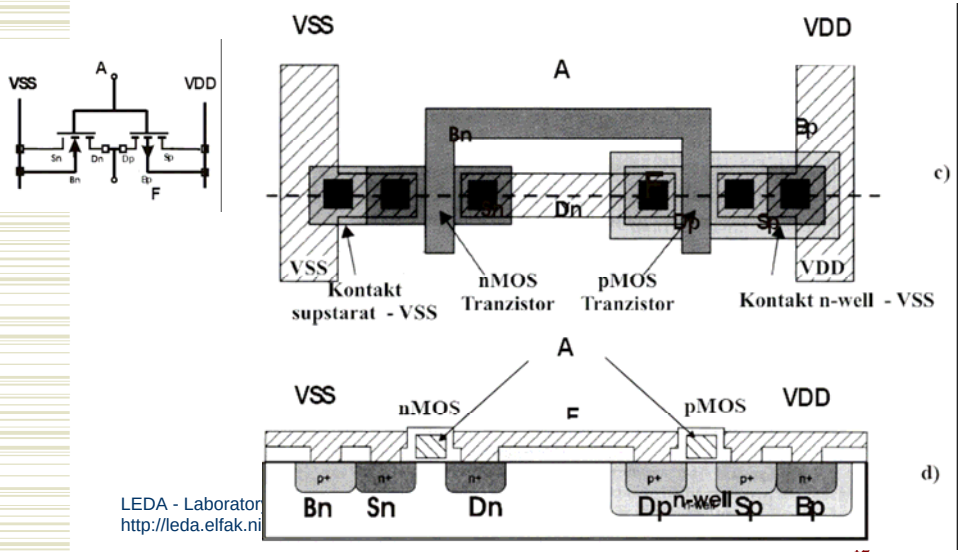

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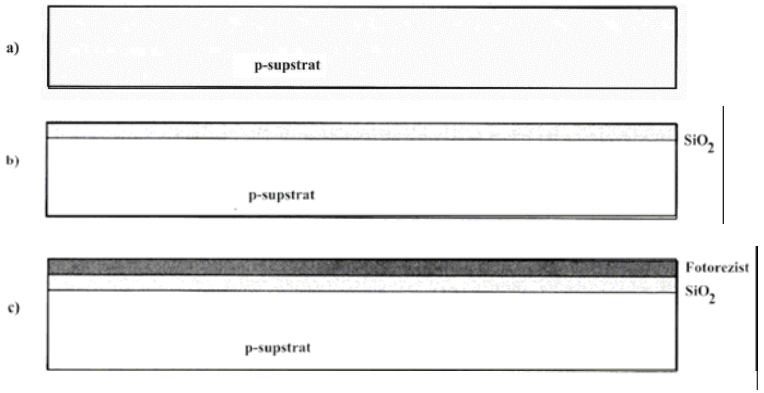

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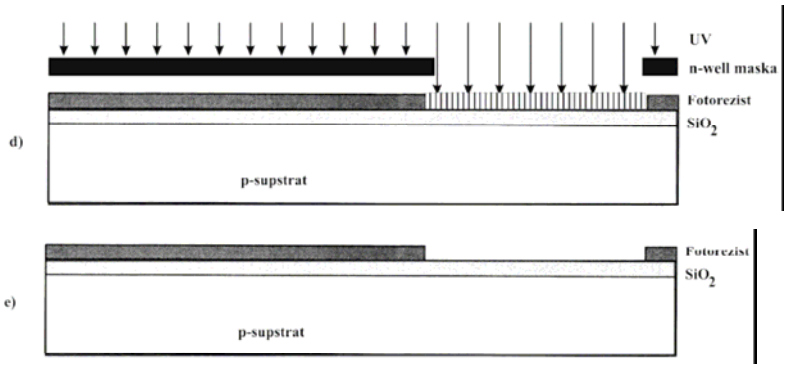

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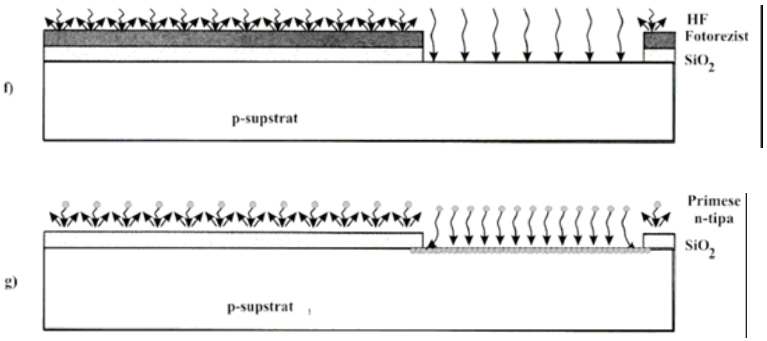

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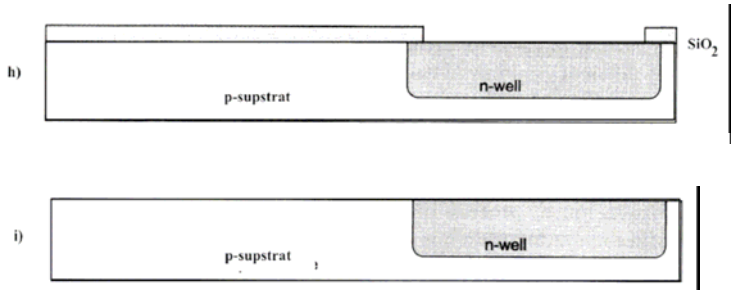

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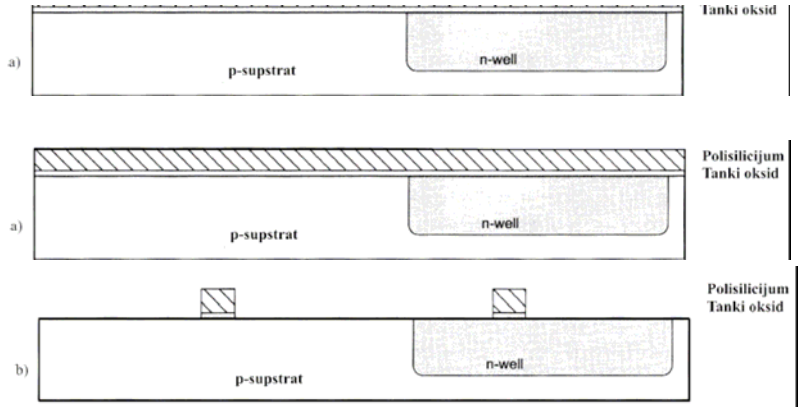

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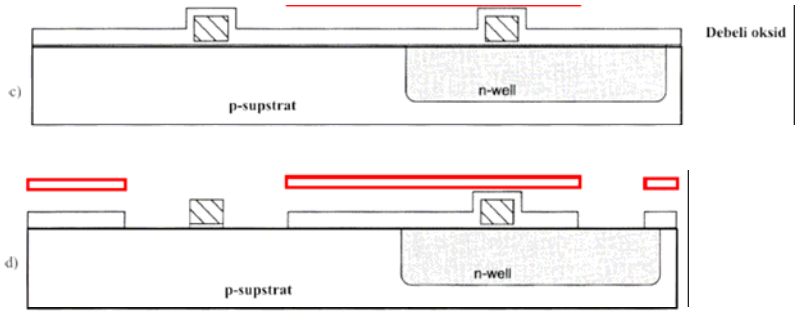

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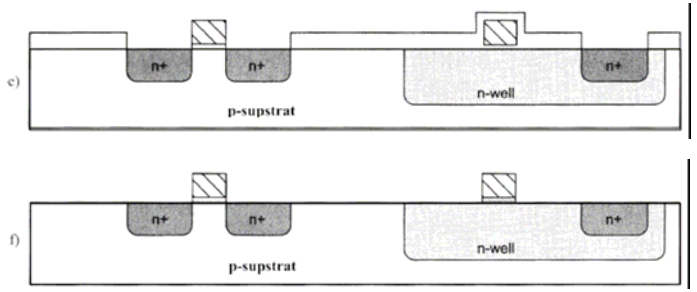

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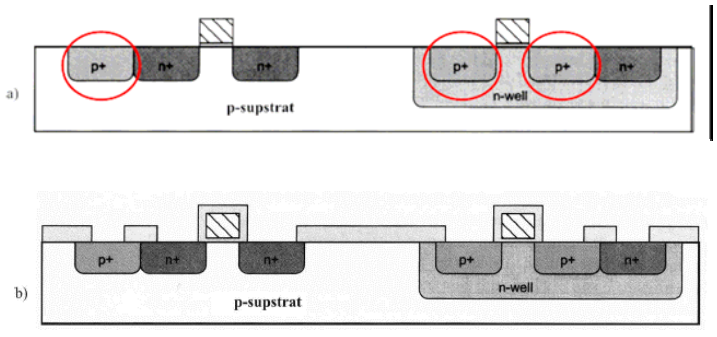

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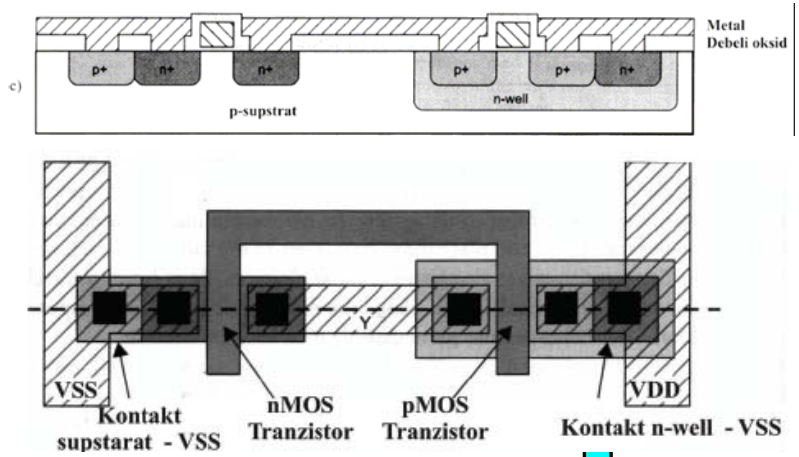

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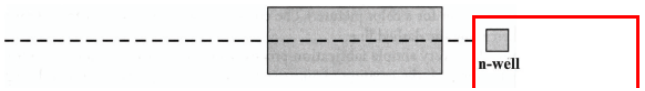

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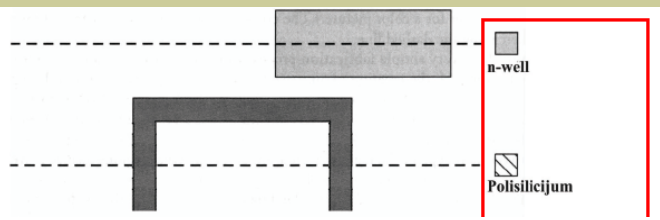

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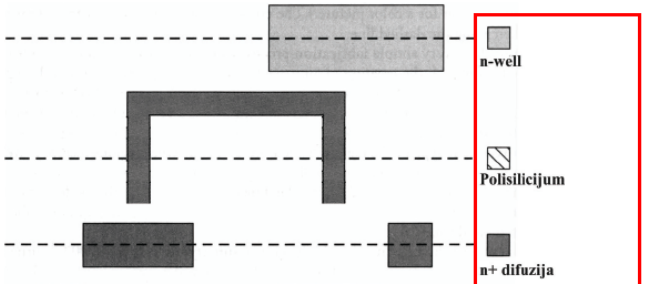

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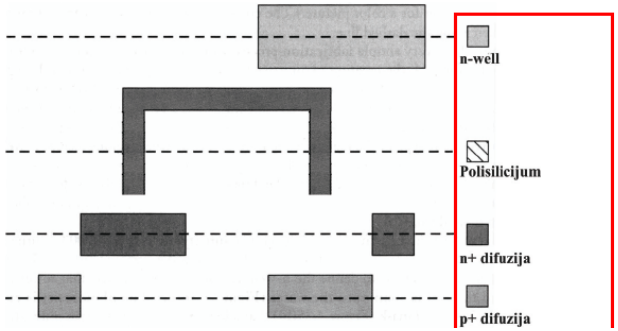

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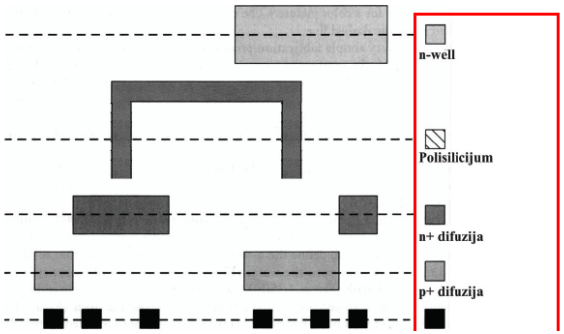
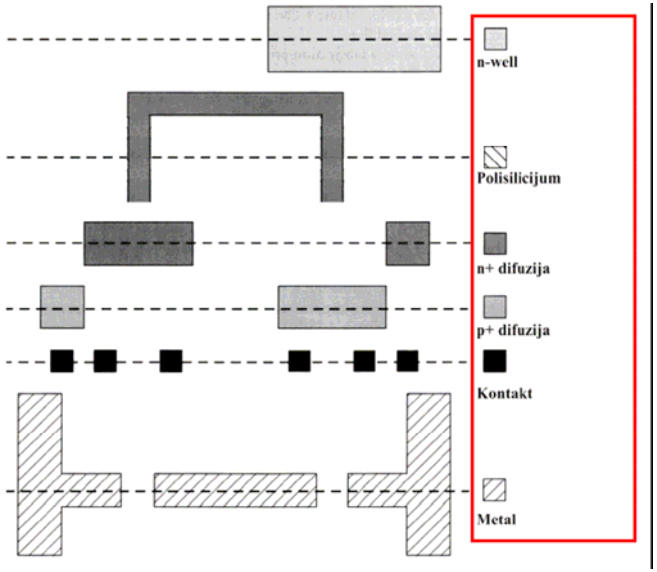


2.1 Osnovni CMOS proces



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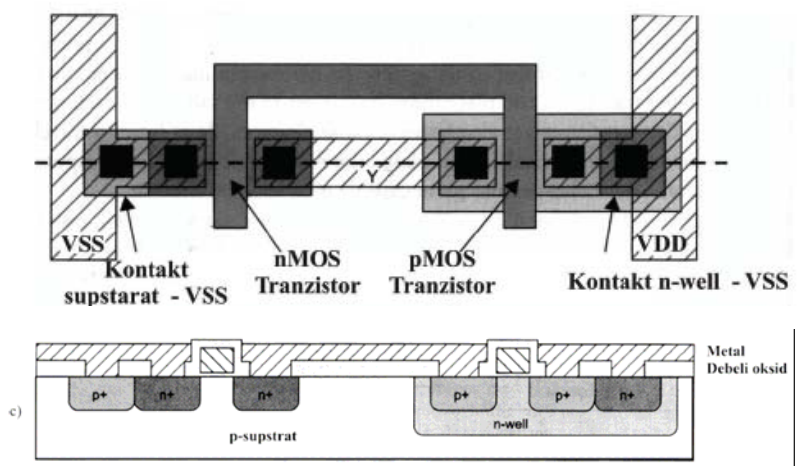


2. CMOS proces

Sadržaj:

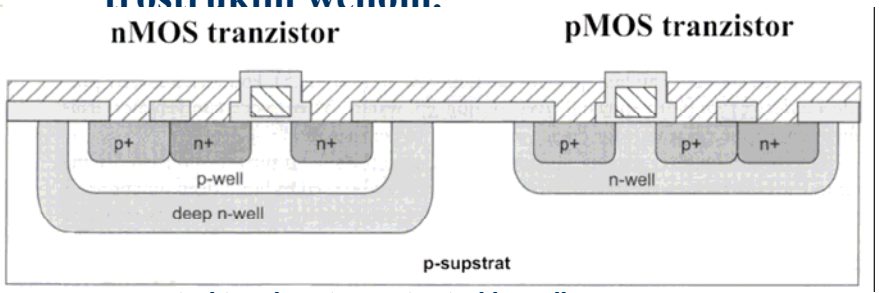
2.2 Submikronski CMOS proces

Savremeni tehnološki procesi komplikovaniji su od opisanog utoliko što se koriste mnogo složeniji profili dopiranja kako bi se obezbedila

- **bolja izolacija,**
- **bolje karakteristike kratkokanalnih tranzistora i**
- **bolje povezivanje.**

2.2 Submikronski CMOS proces

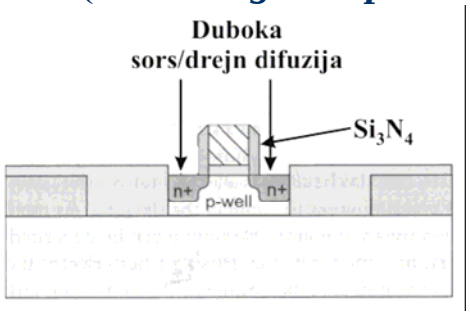
Za bolju izolaciju između tranzistora koriste se postupci sa dvostrukim ili trostrukim wellom.



struktura invertora sa trostrukim wellom.

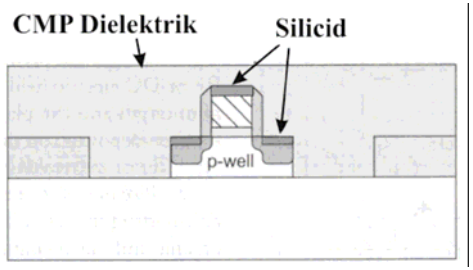
2.2 Submikronski CMOS proces

Da bi se smanjilo električno polje na drejnu (napon je na njemu najveći), koristi se struktura sa slabo dopiranim drejnom (LDD - *Light Doped Drain*).



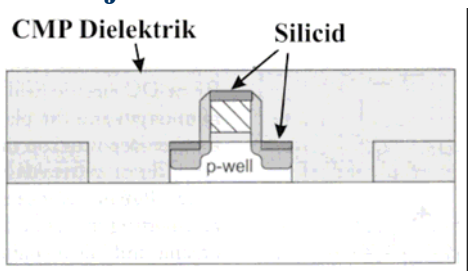
2.2 Submikronski CMOS proces

Da bi se povećala provodnost gejta od polisilicijuma (često se naziva poligejt) i površine sorsa i drejna, koristi se *silicidni* (*silicide*) sloj koji ima smanjenu otpornost.



2.2 Submikronski CMOS proces

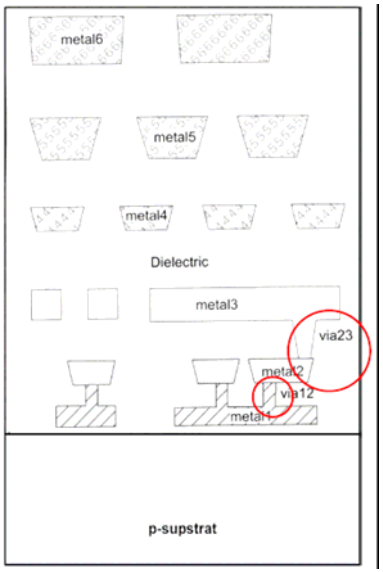
***Chemical Mechanical Polishing* dielektrik primenjuje se kod CMOS procesa koji koriste više metalnih slojeva jer fizički štite, daju čvrstinu i međusobno izoluju metalne veze u višim slojevima.**



2.2 Submikronski CMOS proces

Kod VLSI kola posebno je izražen problem veza.

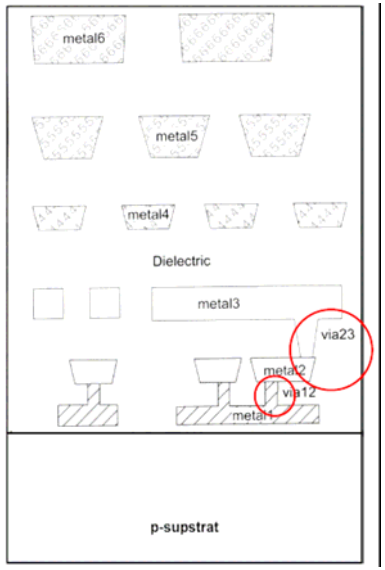
Broj tranzistora na čipu je porastao, tako da su veze postale sve duže (u odnosu na tranzistore).



2.2 Submikronski CMOS proces

Sa druge strane, dimenzije veza su skaliranjem smanjene, tako da im je otpornost, a time i kašnjnje duž veza poraslo.

Pored toga, i potrošnja je porasla pa i dovođenje napajanja zahteva veze drugačijeg profila.



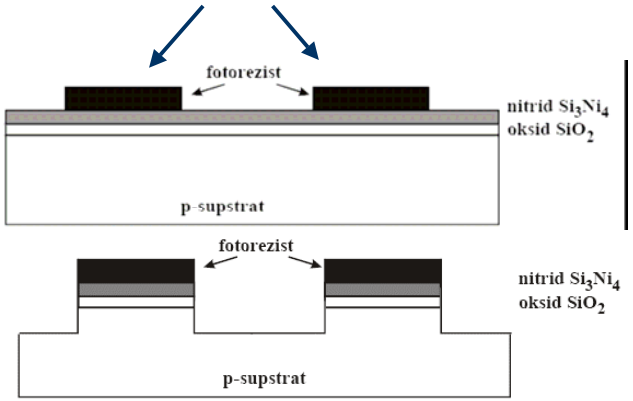
2.2 Submikronski CMOS proces

Savremeni tehnološki procesi dimenzija ispod 0.35µm razlikuju se od osnovnog CMOS procesa u četiri važna detalja jer koriste:

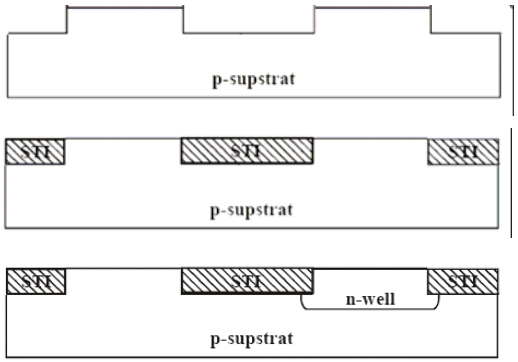
1. plitku ukopanu izolaciju između tranzistora (STI, *Shallow Trench Isolation*)
2. dopirane poligejtove (n+ poli za nMOS i p+ poli za pMOS)
3. LDD za redukovanje efekata kratkih kanala
4. silicid, odnosno salicid za smanjenje parazitnih otpornosti

2.2 Submikronski CMOS proces

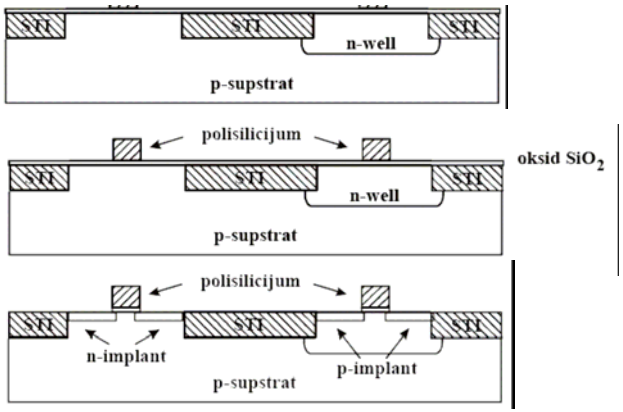
Zaštite se oblasti u kojima će se formirati tranzistori - Aktiv



2.2 Submikronski CMOS proces



2.2 Submikronski CMOS proces



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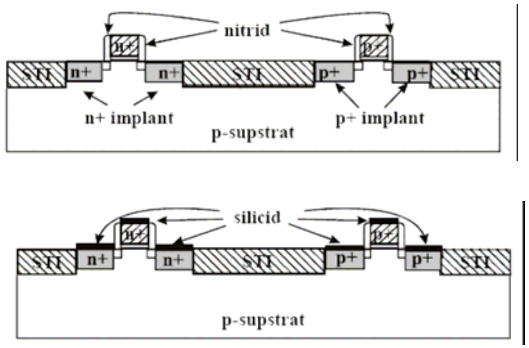

2. CMOS proces

Sadržaj: